Remarks/Arguments

Claims 1-14, including new claims 7-14, remain in this application.

The examiner has objected to claim 6 under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim.

The examiner has rejected claims 1-5 under 35 USC 102(e) as being anticipated by *Dervisoglu, et al.*, United States Published Patent Application 2003/0131327.

In view of the above amendments and these remarks, reconsideration of the above noted rejections and objections is respectfully requested.

Claim Objections:

Due to the above amendments, Applicant respectfully traverses the objection to **claim 6** under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Claim 6 has been amended to depend from claim 5, instead of from claim 4. Claim 5, not claim 4, includes the selecting means that claim 6 further limits to include a multiplexer. Applicant respectfully submits that the amendment to claim 6 cures the grounds for the objection under 37 CFR 1.75(c).

Rejections under 35 USC 102(e):

Applicant respectfully traverses the rejection of claims 1-5 under 35 USC 102(e) as being anticipated by *Dervisoglu, et al.* The independent claims are 1, 2, 4 and 5. Claims 1 and 2 call for "output locations" to which test signals are supplied or passed. Claim 4 calls for "a plurality of output locations at which a portion of the test signals are measured." Claim 5 calls for "a plurality of means for outputting selected ones of the test signals." In each of these cases, the recited "output locations" or "outputting means" are **plural**. Additionally, claims 2, 4 and 5 call for "groups" of the test signals, which means that the test signals are also plural. In other words, claims

1, 2, 4 and 5 call for outputting **plural** test signals in **parallel**. Applicant respectfully submits that *Dervisoglu, et al.* does not teach or suggest the plural "output locations" or "outputting means" and, thus, cannot output plural test signals in parallel.

Dervisoglu, et al. discloses only a **single** output signal TDO 122 at [0043] and in Fig. 1, so the output data must be in serial, rather than in parallel. *Dervisoglu, et al.* also discloses that the chip access port (CAP), the test access port (TAP) and the socket access ports (SAP) comply with IEEE standard 1149.1 (paragraphs [0019], [0043], [0048], [0050] and [0053]), which calls for **serializing** output data. Additionally, *Dervisoglu, et al.* states at [0057] that "Preferably, both the boundary-scan cells (or registers) 240 and the instruction register of the chip access port 205 are loaded and unloaded using **serial access** (i.e., scan) of their contents, via the Test Data Input (TDI) signal pin and Test Data Output (TDO) signal pin, respectively." *Dervisoglu, et al.*, therefore, teaches outputting serialized data at a single output.

Applicant respectfully submits, therefore, that independent claims 1, 2, 4 and 5 are not anticipated by, are not obvious from, and are patentable over *Dervisoglu, et al.*, since the reference does not teach or fairly suggest plural or parallel outputs or test signals as claimed. Additionally, since claims 3 and 6 depend from claims 2 and 5, respectively, claims 3 and 6 also are not anticipated by, are not obvious from, and are patentable over *Dervisoglu, et al.* for the same reasons.

Additional Claim Amendments:

Amendments, not mentioned in the above remarks, have been made to claims 3, 4 and 5 to correct minor errors discovered upon reviewing the Application. In particular, claim 3 has been amended to depend from claim 2, instead of claim 1. It is apparent that the original dependency was an inadvertent error, since the antecedent basis for the reference to "the highest regional level" (in claim 3, at line 3) is found in claim 2 (at line 5), rather than in claim 1. Additionally, claims 4 and 5 have been amended to place a period, instead of a semicolon, at the end of the claims and to add the word "and" before the last limitations of the claims.

New Claims:

New dependent claims 7-14 have been added to the Application. Applicant respectfully submits that these new claims do not add new matter. Specifically, new dependent claims 7, 9, 11 and 13 depend from independent claims 1, 2, 4 and 5, respectively, and introduce the limitation that the test points or test signal generating means are **internal** to circuitry of the IC. The signals generated therein are ordinarily hidden from the I/Os during normal operation of the IC. This limitation is supported in the specification wherein mention is made of "internal signals," "internal test points" and "internal workings." (See p. 1, lines 15, 17, 18 and 24-26; p. 2, lines 1-3, 6, 18, 19; and p. 3, lines 4, 5 and 12.) Additionally, new dependent claims 8, 10, 12 and 14 depend from new dependent claims 7, 9, 11 and 13, respectively, and introduce the limitation that the test signals are **live signals** from the internal test points of the circuitry of the IC. This limitation is supported in the specification wherein mention is made that **the test signals, themselves,** are passed from the test points through the multiplexers to the output locations (p. 5, lines 12-28), where the test signals are measured directly (p. 1, lines 18-19; p. 3, lines 2-5; and p. 6, lines 2-4).

Applicant respectfully submits that *Dervisoglu, et al.* does not teach or fairly suggest the limitation that the test points or test signal generating means are **internal** to circuitry of the IC per claims 7, 9, 11 and 13. Instead, *Dervisoglu, et al.* discloses that the boundary scan cells/registers 124 or 240 get data only from the external I/O pins, not from within the circuitry. (See Figs. 1 and 2 and paragraphs [0045] and [0054].) In other words, the test data output comes not from inside the integrated circuit core 126, but from the normal output signals that the core produces during normal operation, and this data is captured by the boundary scan cells/registers 124 or 240 before being serialized at the chip access port 205 and output at the TDO 122 (Fig. 1).

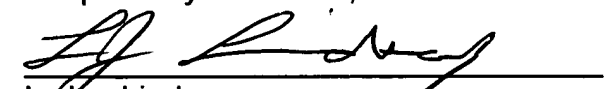
Applicant further respectfully submits that *Dervisoglu, et al.* does not teach or fairly suggest the limitation that the test signals are **live signals** from the internal test

points of the circuitry of the IC per claims 8, 10, 12 and 14. Instead, *Dervisoglu, et al.*, as discussed above, discloses in [0043] and Fig. 1, that it has one signal (test data output (TDO) signal 122) for outputting test data, so the data must be serialized. In order to serialize data, it must be "captured." The data is, thus, captured by the boundary scan cells/registers 124 or 240 before being serialized at the chip access port 205 and output at the TDO. (See paragraphs [0045] and [0055].) *Dervisoglu, et al.*, thus, deals with a serialized stream of captured data, not raw signals measured directly at the outputs. Therefore, the circuitry disclosed in *Dervisoglu, et al.* cannot output "live" data.

For the reasons specifically discussed above, and others, it is believed that pending claims 1-14 define patentable subject matter. Reconsideration of the previous rejections as they might apply to the pending claims is therefore respectfully requested. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

October 13, 2004
Date



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